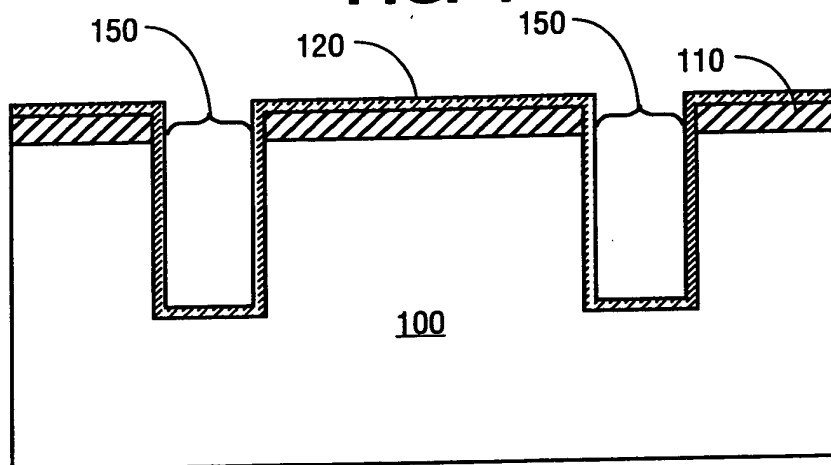
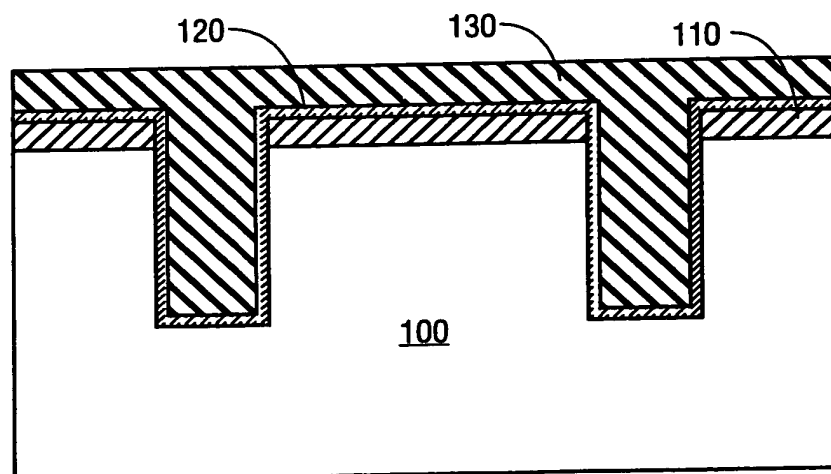


**FIG. 1**



**FIG. 2**

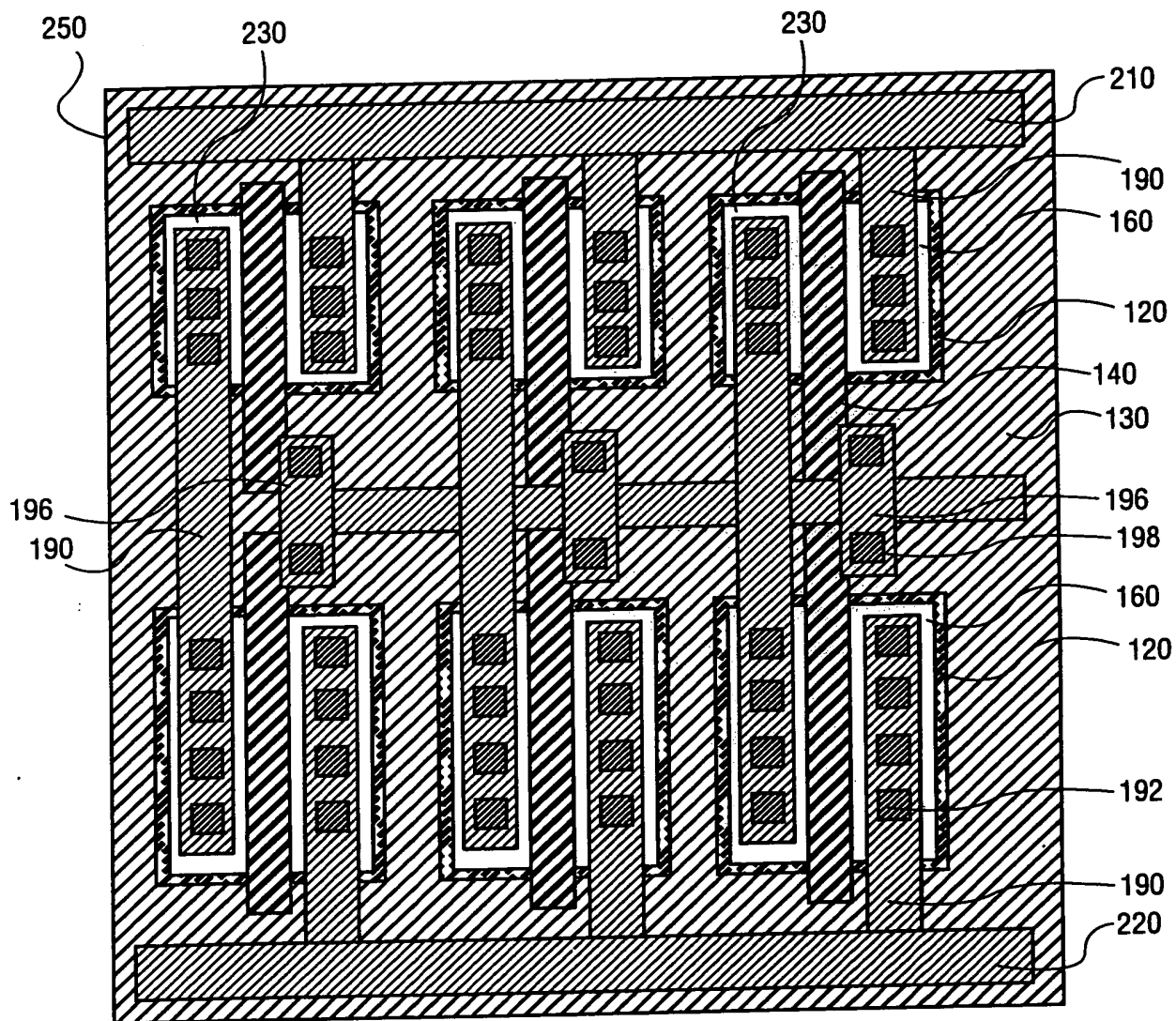


**FIG. 3**

A cross-sectional view of a substrate 100. The substrate has a top surface and a bottom surface. Two rectangular openings are formed in the top surface. Each opening is filled with a material 130, which is shown with diagonal hatching. The openings are separated by a central region of the substrate. A label 120 points to the right side of the substrate.

This cross-sectional view shows a semiconductor device with a central gate structure. The device is built on a substrate 100. A gate stack 120 is formed on the substrate, with a gate dielectric 130 and a gate conductive layer 140. The gate conductive layer 140 is patterned to form a central gate 140. The gate stack 120 is surrounded by a spacer 160. The spacer 160 is formed by a first spacer layer 180 and a second spacer layer 190. The first spacer layer 180 is a conductive layer, and the second spacer layer 190 is an insulating layer. The device is further defined by a top layer 195 and a bottom layer 196. The top layer 195 is a conductive layer, and the bottom layer 196 is an insulating layer. The device is further defined by a top layer 195 and a bottom layer 196.

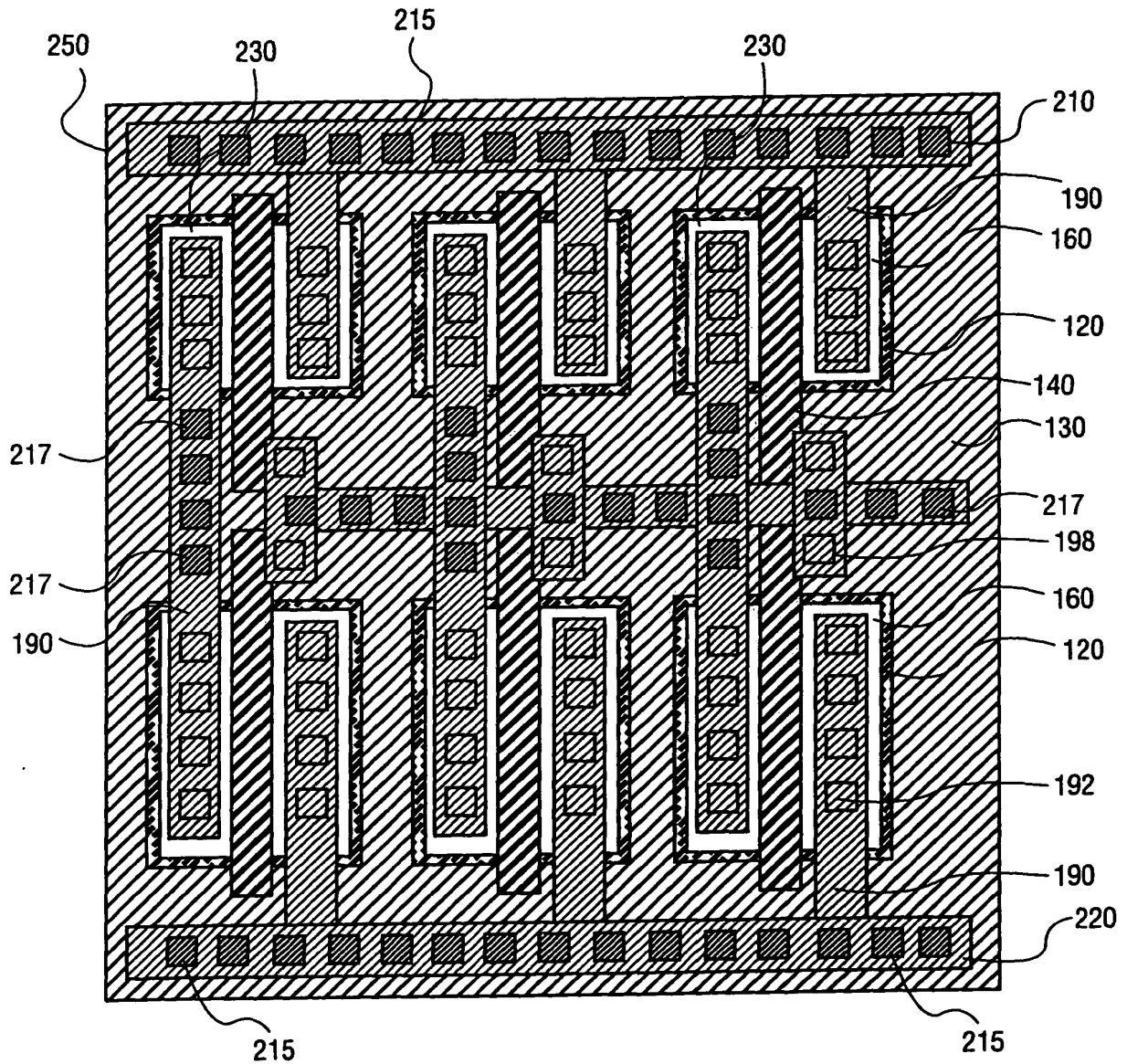
**FIG. 6**



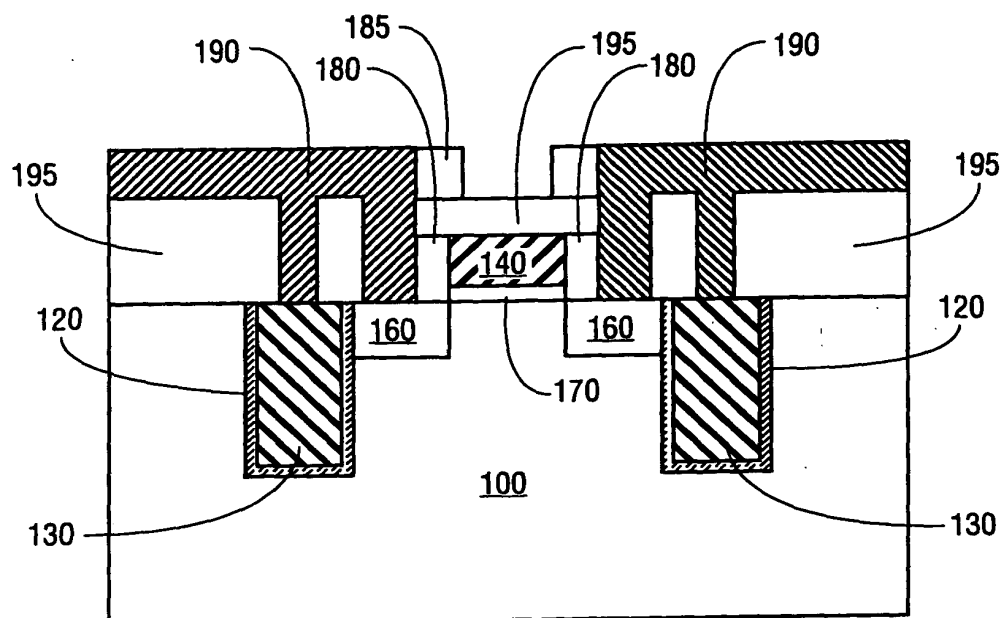
**FIG. 7**



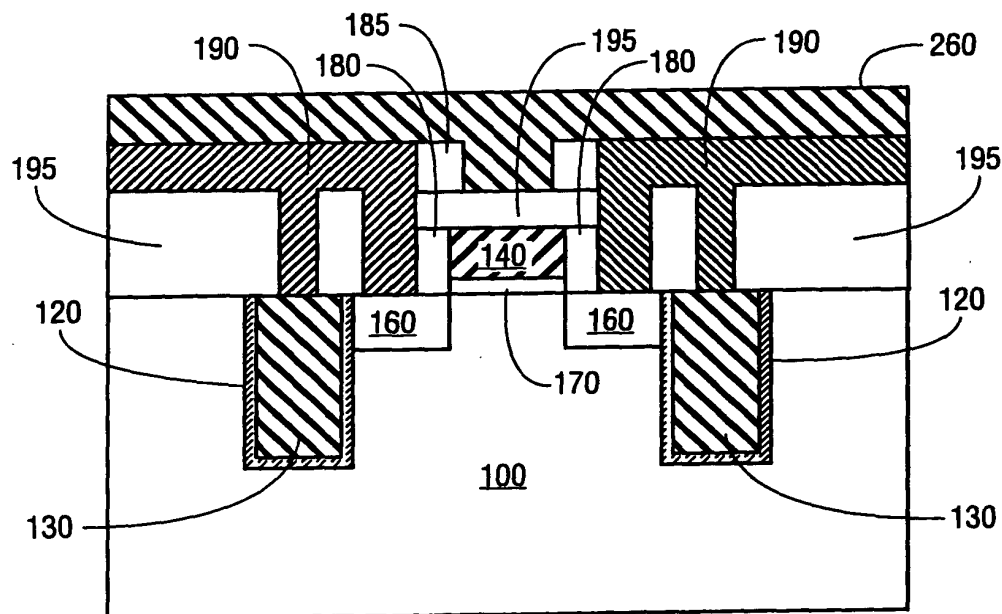
**FIG. 8**



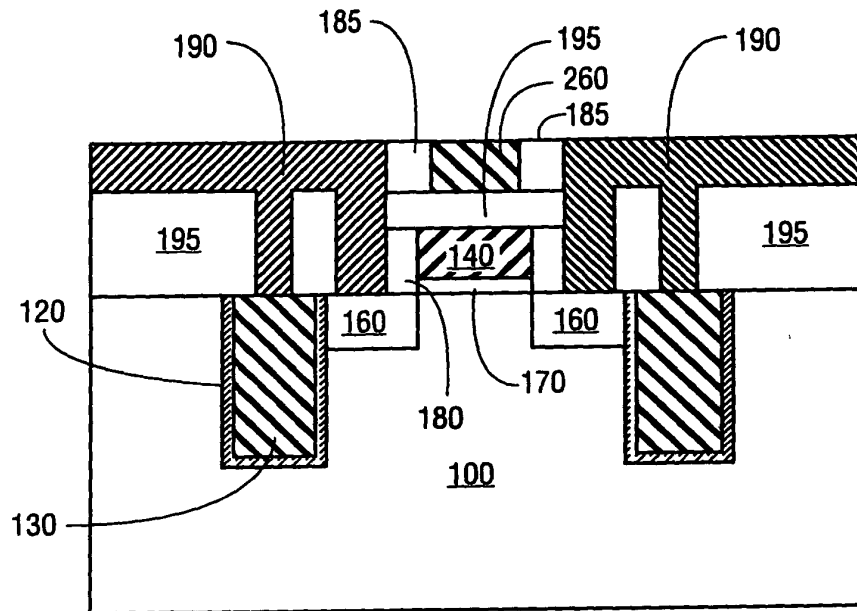
**FIG. 9**



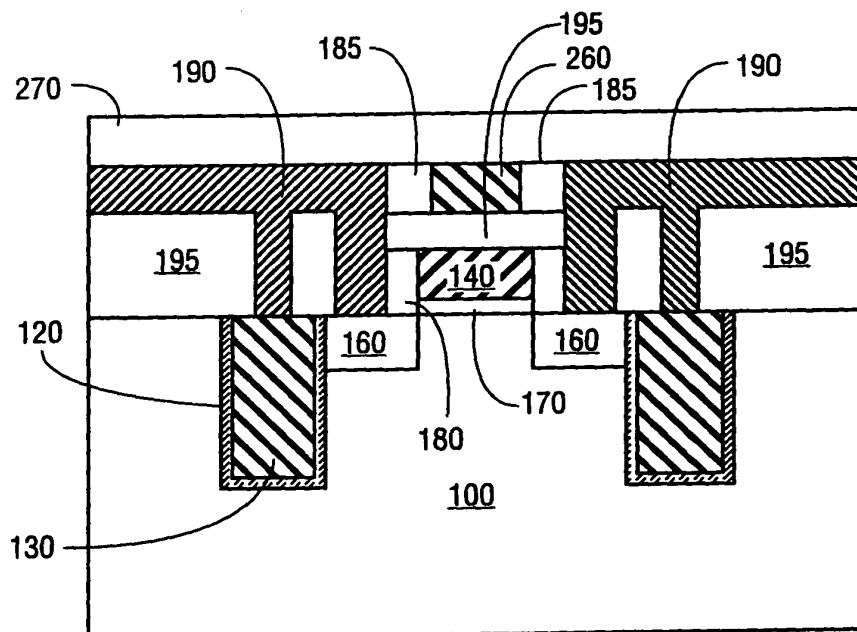
**FIG. 10**



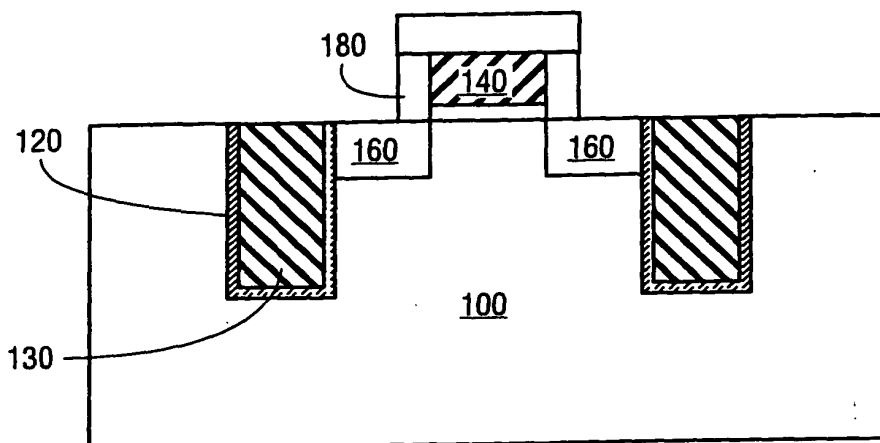
**FIG. 11**



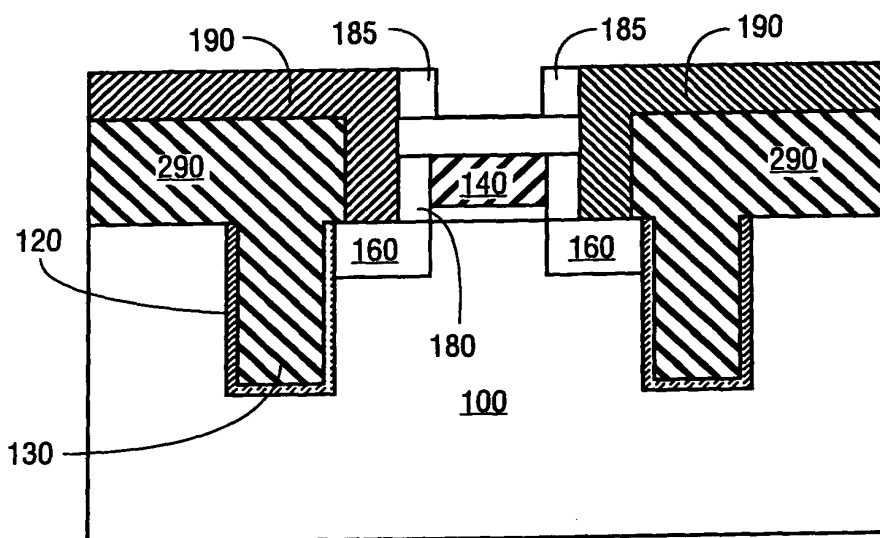
**FIG. 12**



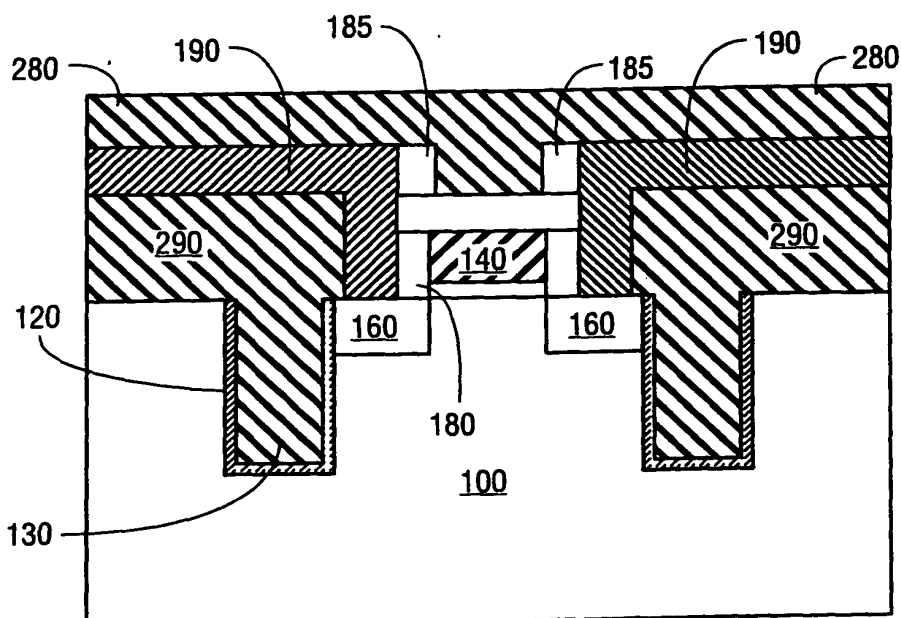
**FIG. 13**



**FIG. 14**



**FIG. 15**



**FIG. 16**